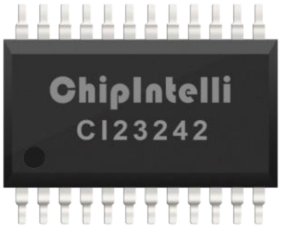
CI23242 Data sheet

High performance neural network intelligent voice chip



- **Brain Neural Network Processor (BNPU)**

--BNPU V3.5, supports DNN\TDNN\RNN\CNN and other neural networks and parallel vector operations, can achieve high performance speech recognition and speech noise reduction functions

CPU and memory

--CPU frequency up to 210 MHz

--Built-in 2MBytes Flash memory

-Built-in 288KBytes SRAM

－ Built-in 256-bit eFuse for application encryption

- **Audio Codec**

-High performance low power consumption audio ADC, SNR ≥ 95dB

--Low power consumption audio DAC, SNR ≥ 95dB

- **PWM**

-Supports 4 PWM interfaces

- **GPIO**

--11-way high-speed GPIO with a flip frequency of up to 20MHz

--5 GPIO channels support 5V level communication

- **Reset and power management**

-Supply voltage range 3.6V～5.5V

-Built-in PMU power management unit

-Built-in power-on reset (POR)

-Built-in voltage detection (PVD)

- **Clock**

-Built-in RC oscillator

-Bluetooth external crystal oscillator input

- **Communication interface**

-1 IIC interface

-2 UART interfaces, support 5V level communication, up to 3Mbps communication rate

- **Timer and watchdog**

-Built-in 2 sets of 32-bit timers and 1 watchdog

- Wireless features

- BLE 5.4

- +5 dBm Max TX power

-98 dBm RX sensitivity@ BLE 1 Mbps

catalogue

1 Summary

1.1 Functional description

The CI2324X is a next-generation high-performance neural network smart voice Bluetooth chip developed by Chipintelli, integrating the company's proprietary Brain Neural Network Processor (BNPU) V3.5 and CPU core. With a system clock rate of up to 210MHz, it features 288KB of built-in SRAM, a PMU power management unit, and an RC oscillator. The chip incorporates a single-channel high-performance low-power Audio Codec along with multiple peripheral control interfaces including UART, I2C, PWM, and GPIO, while also supporting high-performance low-power Bluetooth (BLE). Remarkably, the CI2324X requires only minimal external components like resistors and capacitors to implement hardware solutions for various smart voice products, delivering exceptional cost-effectiveness.

CI2324X adopts industrial design standards, has good environmental reliability, its working temperature range-40℃ ～+85℃, in line with MSL3 grade of moisture sensitivity, in line with IEC 61000-4-2 of 4KV contact discharge test standard, in line with RoHS and REACH environmental protection standards.

The CI2324X leverages Chipintelli's next-generation BNPU technology, which supports neural networks (DNN/TDNN/RNN/CNN) and parallel vector operations, enabling high-performance speech recognition, noise reduction, and exceptional environmental noise suppression capabilities. It also features Bluetooth BLE 5.4 transceiver support for remote device control via mobile mini-programs. The CI2324X solution supports multiple global languages including Chinese, English, and Japanese, making it ideal for smart home appliances, lighting systems, toys, wearables, industrial applications, and automotive products. This platform facilitates voice interaction controls and diverse intelligent voice application scenarios.

1.2 Chip specifications

The function block diagram of CI23242 is shown in Figure 1-1:

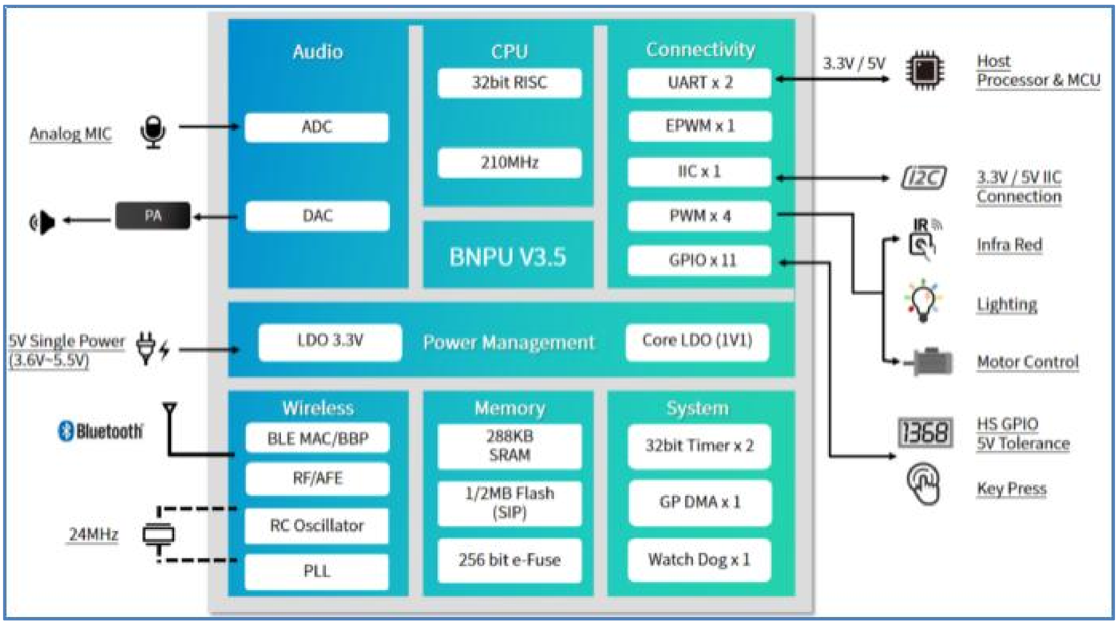


Figure 1-1 CI23242 function block diagram

- **Brain network processor BNPU V3.5**

-It adopts the new generation of Chipintelli hardware BNPU technology, supports DNN\TDNN\RNN\CNN and other neural networks and parallel vector operations, and can realize high performance speech recognition, speech noise reduction and other functions

- **CPU**

-32-bit high performance CPU, up to 210MHz operating frequency

- **Memory**

-Built-in 288KB SRAM

-Built-in 256bit eFuse

-Built-in 2MB Flash

- **PDA**

-Bluetooth 5.4

- +5 dBm Max TX power

-98 dBm RX sensitivity@ BLE 1 Mbps

- **Audio interface**

-Built-in high performance low power Audio Codec module, support single channel ADC sampling and single channel DAC playback

-Support for Automatic Level Control (ALC)

-Support for 8kHz/16kHz/24kHz/32kHz/44.1kHz/48kHz sampling rate

- **Power management unit PMU**

-Support wide power supply voltage, power supply range 3.6V～5.5V

-Built-in 2 high performance LDO circuits, no need to configure external power chip, application scheme only needs a small number of peripheral components

- **Clock**

-Built-in RC oscillator

-Bluetooth external crystal oscillator input

- **External devices and timers**

-2 UART interfaces, support up to 3M baud rate communication

-1 IIC interface, which can be connected to IIC devices for expansion

-4 PWM interfaces, which can be directly driven for lamp control and motor applications

-Built-in 2 sets of 32bit timers

-Built-in 1 independent watchdog (IWDG)

- **GPIO**

-Supports 11 GPIO ports and can be used as a master control IC

-Each GPIO port can be configured with interrupt function and pull-up/down state

-5GPIO channels can directly support 5V level communication through an external 5V pull-up resistor

- **Software development support**

-Provide complete software development kits, application solution examples, direct online firmware development using the voice development platform and other support. For details, please visit: https://aiplatform.chipintelli.com

- **Firmware burning and protection**

-Support UART upgrade and firmware protection

- **ESD function**

-Internal ESD enhanced design, can pass 4KV contact discharge test

- **ROHS and REACH**

-Use of environmentally friendly materials, support RoHS and REACH standards

- **Encapsulation and operating temperature range**

-Packaging form: SSOP24, size of 8.6mm long, 6.0mm wide and 1.75mm high

-Working environment temperature: -40℃ ～+85℃

2 Pin diagram and function description

2. 1 Pin diagram

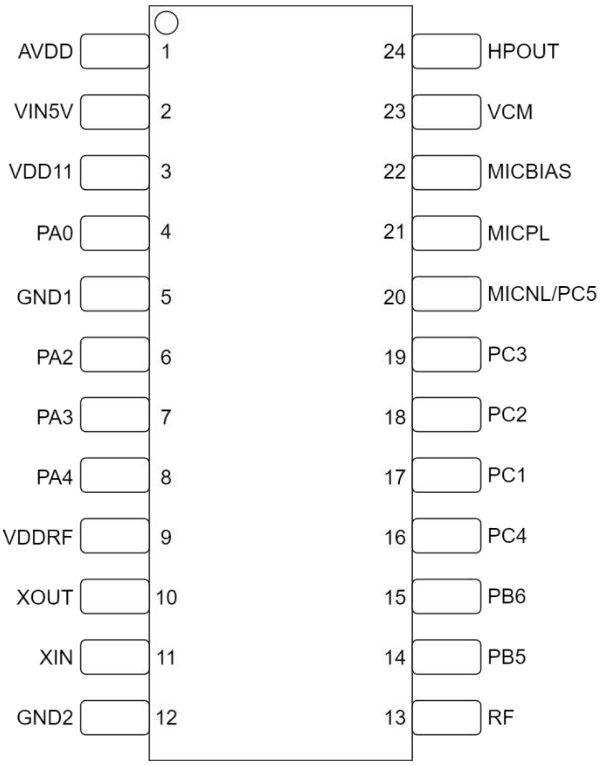


Figure 2-1 CI23242 pin sequence and definition Figure

2. 2 Pin Description

Pin description Table 2-1

Pin Number	Pin Name	Type	5V Tolerant	Power-on Default State	Pin Function
1	AVDD	P	-	-	● Internal LDO-3.3V output ● Internal analog circuit 3.3V power supply input * Note1*
2	VIN5V	P	-	-	● Power supply voltage input, power supply voltage range 3.6V～5.5V * Note1*
3	VDD11	P	-	-	● LDO-1.1V output ● The kernel has a 1.1V power supply input * Note1*
4	XIN	IO	-	-	● External clock input ● GPIO PA0 ● PWM2
5	GND	P	-	-	● Ground
6	PA2	IO	√	IN，T+D	● GPIO PA2 (default state on power up) ● IIC_SDA ● PWM0 ● PWMP
7	PA3	IO	√	IN，T+D	● GPIO PA3 (default state on power up) ● IIC_SCL ● PWM1 ● PWMN
8	PA4	IO	√	IN，T+U	● GPIO PA4 (default on power) /PG_EN * Note2* ● PWM2 ● PWMP
9	VDDRF	P	-	-	● RF power input ● * Note1*
10	XOUT	IO	-	-	● Jingzhen outputs* Note4*
11	XIN	IO	-	-	● Jewel input* Note4*
12	GND	P	-	-	● Ground
13	RF	IO	-	-	● RF antenna
14	PB5	IO	√	IN，T+U	● GPIO PB5 (default on power up) ● UART0_TX ● IIC_SDA ● PWM1 ● PWMP
15	PB6	IO	√	IN，T+U	● GPIO PB6 (default on power up) ● UART0_RX ● IIC_SCL ● PWM2 ● PWMN
16	PC4	IO	-	IN,T+U	● Retained (default state on power-on) ● PC4 ● SCL ● PWM0
17	PC1	IO	-	IN,T+D	● Retained (default state on power-on) ● PC1

					● TX2 ● PWM3
18	PC2	IO	-	IN,T+U	● Retained (default state on power-on) ● PC2 ● RX2 ● PWM2
19	PC3	IO	-	IN,T+D	● Retained (default state on power-on) ● PC3 ● SDA ● PWM1
20	MICN/PC5	IO	-	IN,T+D	● Microphone N input ● Retained (default state on power-on) ● PC5 ● BOOT* Note3*
21	MICP	I	-	-	● Microphone P input
22	MICBIAS	O	-	-	● Microphone bias output
23	VCM	O	-	-	● VCM POWER Output
24	HPOUT	O	-	-	● DAC output

Note1: The pin needs to be connected to a 4.7uF capacitor

Note2: This pin is high level when powered on, and the system will enter programming mode

Note3: The pin cannot be pulled up during power on, otherwise the system will enter debug mode

Note4: Pin10 XOUT and Pin11 XIN are Bluetooth crystal input/output pins, which only provide clock for Bluetooth; the voice clock is provided by the built-in RC oscillator of the chip

Symbol definition ：

I import　I import

O output　O output

IO two-way　IO two-way

P Power or ground　P Power or ground

T+D three-state down　T+D three-state down

T+U Tri-State Pull-Up T+U Tri-State Pull-Up

OUT The default output of the power supply　OUT The default output is on

IN Upper default input IN Upper default input

All IOs can be configured with drive capability and pull-up/down status.

2. 3 IO Multiplexing Functionality

Table 2-2 IO multiplexing functions

Pin Name	Function1	Function2	Function3	Function4	Function5	Function6	Specific Function
XIN	PA0	PWM2	-	-	-	-	XIN
PA2	PA2	-	IIC_SDA	-	PWM0	PWMP	-
PA3	PA3	-	IIC_SCL	-	PWM1	PWMN	-
PA4	PA4	-	-	-	PWM2	-	PG_EN *Note5*
PB5	PB5	UART0_TX	IIC_SDA	PWM1	PWMP	-	-
PB6	PB6	UART0_RX	IIC_SCL	PWM2	PWMN	-	-
PC1	-	PC1	TX2	PWM3	-	-	-
PC2	-	PC2	RX2	PWM2	-	-	-
PC3	-	PC3	SDA	PWM1	-	-	-
PC4	-	PC4	SCL	PWM0	-	-	ICE
PC5	-	PC5	-	-	-	-	BOOT *Note3*

Note3: The pin cannot be pulled up during power on, otherwise the system will enter debug mode.

Note 5: The PA4 (PG_EN) pin is configured with an internal default pull-up. When the system detects a high-level signal on this pin during power-on and receives a firmware upgrade command from the UART0 interface, it automatically enters upgrade mode, allowing programming of the chip's internal Flash memory through the upgrade tool. If no firmware upgrade command is detected on the UART0 interface or if the PA4 pin voltage remains low, the system will revert to normal operation mode.

3 Electrical character

Table 3-1 Electrical characteristics table

Symbol	Description	Min	Typ	Max	Unit
VIN5V	Chip power input *Note6*	3.6	5.0	5.5	V
AVDD	3.3V power supply	2.97	3.3	3.63	V
VDD11	1.1V power supply	0.99	1.1	1.21	V
VIH	Enter a high level （3.0V ≤VDD33 ≤ 3.6V）	0.7×VDD33	-	VDD33+0.3	V
VIL	Input low level （3.0V ≤ VDD33 ≤ 3.6V）	-0.3	-	0.3×VDD33	V
VOL	Output low level @IOL = 12mA	-	-	0.4	V
VOH	Output high level @IOH = 20mA	2.4	-	-	V
I5V-IO	Drive current at 3.3V when the 5V voltage IO port is output	20	-	33	mA
I3V3-IO	3.3V voltage withstand IO output 3.3V drive current	14	-	24	mA
ΣIVDD	The sum of all the total currents of the chip	-	-	260	mA
Pde	The chip uses 5V power supply and VDD11 uses external supply 1.1V state. The total power consumption of 5V power supply (TA = 25 ° C) is normal when recognized	80	-	140	mW
Pdi	The chip is powered by 5V and the system is powered by internal LDO. The total power consumption of the 5V input (TA = 25 ° C) is normally recognized	160	-	310	mW
Precision of RC oscillator *Note7*	TA：-40℃～+85℃	-1.5	-	+1.5	%
Top	Chip operating temperature	-40	-	+85	℃
Tst	Chip storage ambient temperature	-55	-	+150	℃

Note6: The ripple is required to be less than 300mVp-p.

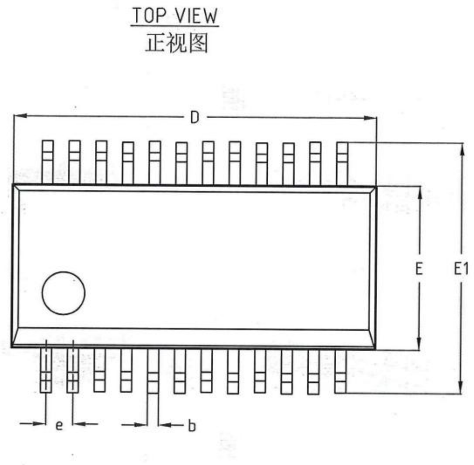
Note 7: Due to the inherent characteristics of semiconductor technology, the built-in RC oscillator in chips may exhibit temperature-dependent frequency drift (±1.5%) under extreme temperatures. The CI23242 chip incorporates a baud rate self-adaptive circuit that ensures stable communication with host computers in varying ambient conditions. For applications requiring ultra-precise clock synchronization, please utilize our externally crystal-configured chips and corresponding implementation solutions.

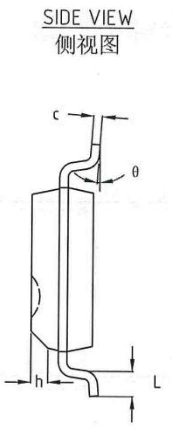
Table 3-2 Bluetooth characteristics table

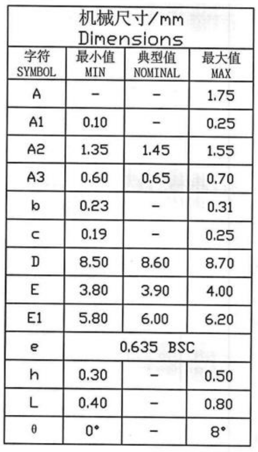
No	Parameter	Symbol	Conditions	MIN	TYP	MAX	UNIT
1	Sleep Power	I_SLEEP	VDDRF=3.3V		6		uA
2	Current in TX 0dBm	I_TX	VDDRF=3.3V		2.5		mA
3	Current in RX 1Mbps BLE	I_RX	VDDRF=3.3V @ -98 dBm sensitivity		2.8		mA
4	Frequency range	Freq		2400		2483.5	Mhz
5	Output power	Pout		-20		5	dBm

The above power consumption data is measured when VDDRF equals 3.3V

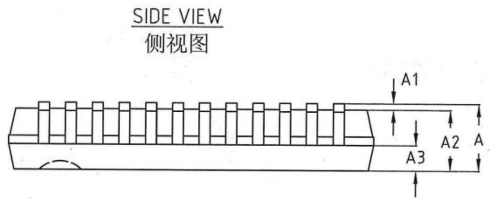
4 Packaging information







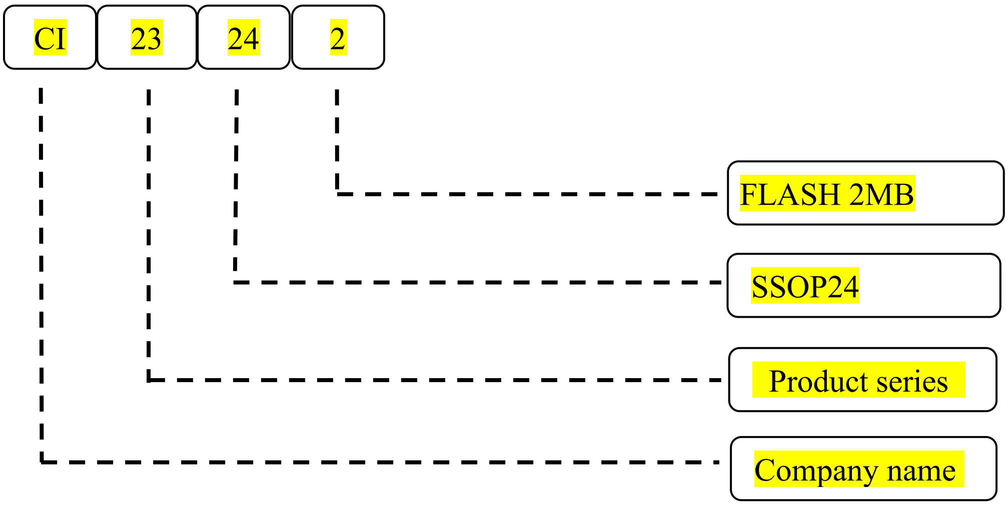
机械尺寸/mm Dimensions			
字符 SYMBOL	最小值 MIN	典型值 NOMINAL	最大值 MAX
A	–	–	1.75
A1	0.10	–	0.25
A2	1.35	1.45	1.55
A3	0.60	0.65	0.70
b	0.23	–	0.31
c	0.19	–	0.25
D	8.50	8.60	8.70
E	3.80	3.90	4.00
E1	5.80	6.00	6.20
e	0.635 BSC		
h	0.30	–	0.50
L	0.40	–	0.80
θ	0°	–	8°



5 Order information

The packaging MRAK of CI23242 chip is shown in the figure below. The first line is the company LOG, the second line is the chip model, the third line is the production batch number, and the dot in the lower left corner is the identification of pin 1.

The chip model is defined as follows:



The order information of CI23242 chip is shown in Table 5-1.

Table 5-1 CI23242 chip order information table

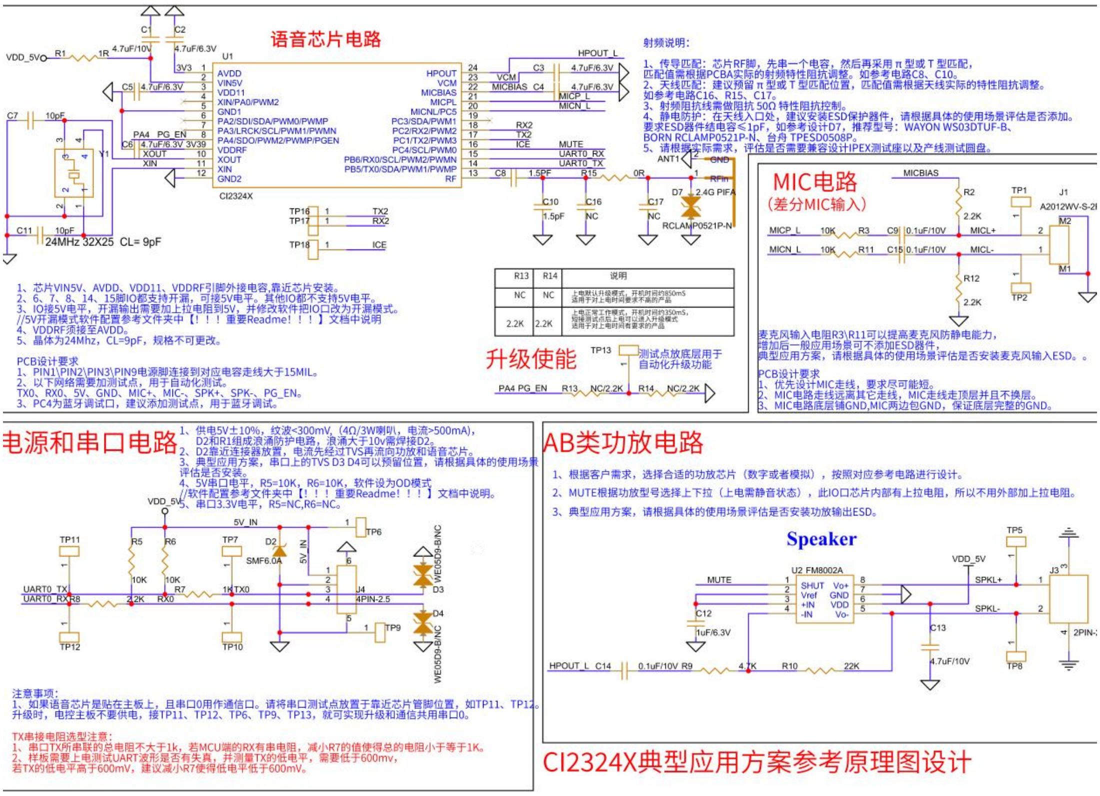
product model	Encapsulation form	Basic packaging	Number of tubes installed	Factory standard package	Standard package quantity
CI23242	SSOP24	piping and instrumentation	50pcs	box-packed	10000pcs (200 tubes/box)

6 Application

6.1 Application reference circuit diagram

The CI2324X chip requires minimal peripheral components to develop terminal product solutions supporting various voice applications. This chip supports single-microphone differential or single-ended input configurations. Application design can select appropriate circuit designs based on functional requirements, power consumption, and cost considerations.

The following is an example of the typical application scheme of CI23242 to introduce the key points and precautions of the application scheme design:



1、芯片VIN5V、AVDD、VDD11、VDDRF引脚外接电容,靠近芯片安装。
2、6、7、8、14、15脚IO都支持开漏，可接5V电平。其他IO都不支持5V电平。
3、IO接5V电平，开漏输出需要加上拉电阻到5V，并修改软件把IO口改为开漏模式。
//5V开漏模式软件配置参考文件夹中【！！！重要Readme！！！】文档中说明
4、VDDRF须接至AVDD。
5、晶体为24Mhz，CL=9pF，规格不可更改。

PCB设计要求
1、PIN1\PIN2\PIN3\PIN9电源脚连接到对应电容走线大于15MIL。
2、以下网络需要加测试点，用于自动化测试。
TX0、RX0、5V、GND、MIC+、MIC-、SPK+、SPK-、PG_EN。
3、PC4为蓝牙调试口，建议添加测试点，用于蓝牙调试。

射频说明：
1、传导匹配：芯片RF脚，先串一个电容，然后再采用π型或T型匹配，
匹配值需根据PCBA实际的射频特性阻抗调整。如参考电路C8、C10。
2、天线匹配：建议预留π型或T型匹配位置，匹配值需根据天线实际的特性阻抗调整。
如参考电路C16、R15、C17。
3、射频阻抗线需做阻抗 50Ω 特性阻抗控制。
4、静电防护：在天线入口处，建议安装ESD保护器件，请根据具体的使用场景评估是否添加。
要求ESD器件结电容≤1pF，如参考设计D7，推荐型号：WAYON WS03DTUF-B、
BORN RCLAMP0521P-N、台舟 TPESD0508P。
5、请根据实际需求，评估是否需要兼容设计IPEX测试座以及产线测试圆盘。

R13	R14	说明
NC	NC	上电默认升级模式，开机时间约850mS 适用于对上电时间要求不高的产品
2.2K	2.2K	上电正常工作模式，开机时间约350mS， 短接测试点后上电可以进入升级模式 适用于对上电时间有要求的产品

测试点放底层用于自动化升级功能

麦克风输入电阻R3\R11可以提高麦克风防静电能力，
增加后一般应用场景可不添加ESD器件，
典型应用方案，请根据具体的使用场景评估是否安装麦克风输入ESD。。

PCB设计要求
1、优先设计MIC走线，要求尽可能短。
2、MIC电路走线远离其它走线，MIC走线走顶层并且不换层。
3、MIC电路底层铺GND,MIC两边包GND，保证底层完整的GND。

1、供电5V±10%，纹波<300mV,（4Ω/3W喇叭，电流>500mA),
D2和R1组成浪涌防护电路，浪涌大于10v需焊接D2。
2、D2靠近连接器放置，电流先经过TVS再流向功放和语音芯片。
3、典型应用方案，串口上的TVS D3 D4可以预留位置，请根据具体的使用场景评估是否安装。
4、5V串口电平，R5=10K，R6=10K，软件设为OD模式
//软件配置参考文件夹中【！！！重要Readme！！！】文档中说明。
5、串口3.3V电平，R5=NC,R6=NC。

注意事项：
1、如果语音芯片是贴在主板上，且串口0用作通信口。请将串口测试点放置于靠近芯片管脚位置，如TP11、TP12。
升级时，电控主板不要供电，接TP11、TP12、TP6、TP9、TP13，就可实现升级和通信共用串口0。

TX串接电阻选型注意：
1、串口TX所串联的总电阻不大于1k，若MCU端的RX有串电阻，减小R7的值使得总的电阻小于等于1K。
2、样板需要上电测试UART波形是否有失真，并测量TX的低电平，需要低于600mv，
若TX的低电平高于600mV，建议减小R7使得低电平低于600mV。

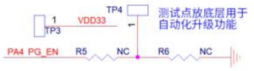
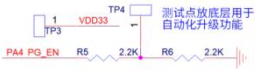
1、根据客户需求，选择合适的功放芯片（数字或者模拟），按照对应参考电路进行设计。
2、MUTE根据功放型号选择上下拉（上电需静音状态），此IO口芯片内部有上拉电阻，所以不用外部加上拉电阻。
3、典型应用方案，请根据具体的使用场景评估是否安装功放输出ESD。

Figure 6-1 Typical application scheme reference circuit diagram of CI2324X

The diagram above shows a reference circuit design for a typical application scenario featuring the CI2324X series chips (including CI23242), which combines single-microphone differential input with power amplifier output. This design is not limited to specific end products. The application solution should be developed based on compatibility with host computer terminal products, and reference schematics and PCB layouts can be downloaded from the Chipintelli Documentation Center and AI Platform according to the functional and performance requirements of the terminal device. Documentation Center link: https://document.chipintelli.com/

If the board-level upgrade function needs to be reserved during the application scheme design, UART0 pins can be led out as sockets or test points, so that the firmware can be burned or upgraded through UART0 after the PCB board is soldered.

The PA4 (PG_EN) pin on CI23242 chip is preconfigured with a 3.3V pull-up resistor. During power-on, the system checks if this pin is set to a high level. If both conditions are met – a high-level signal and an external upgrade command received via UART0 – the system enters upgrade mode. When connected to a pull-down resistor to ground, the chip skips the upgrade detection phase and directly enters normal startup mode, enabling rapid boot-up. For applications requiring fast boot-up, the PA4 pin can be externally connected with two 2.2KΩ pull-down resistors to ground, maintaining a test point between them (refer to reference application diagrams or consult our FAE for detailed implementation). This configuration enables normal startup mode during power-on, reducing boot time to approximately 350ms. To enable online upgrades, a 3.3V high-level signal can be applied through the test point between the two 2.2KΩ resistors to elevate the PA4 pin voltage, allowing UART0 port-based upgrades. The operational modes of PG_EN are summarized in the table below:

PG_EN External resistor diagram	Installation status of R5\R6	PG_EN high and low levels	available machine time
	R5\R6 both NC	High level, upgrade mode	850ms
	R5\R6 贴 2.2K	Low level, working mode	350ms

The CI23242 supports both differential and single-ended microphone inputs, with the differential microphone design shown in Figure H-1 being recommended. For cost-effective implementations, a single-ended microphone input configuration can be adopted to minimize components on the microphone input circuit. However, this approach is only recommended for systems where the microphone input line length is less than 20 centimeters. Longer input lines may impair electromagnetic interference resistance, potentially degrading speech recognition performance.

The power amplifier configuration of this typical application scheme is AB class power amplifier, and the 8002 series power amplifier is recommended. If the voice broadcast function is not required, the circuit can be removed to reduce the cost of the scheme.

If the application scheme does not require ultra-low power consumption, it is recommended that the design scheme use the PMU power supply in CI23242 to reduce the cost. If the application scheme requires ultra-low power consumption, an external DCDC circuit can be used to supply 1.1V power to CI23242 to reduce the system power consumption.

The UART0 of CI23242 supports 5V level communication. If the application scheme needs to be connected to 5V communication level, a 5V pull-up resistor can be added around the RX and TX pins of UART0 without configuring the level conversion circuit.

The crystal specification of CI23242 is 24MHZ, CL is 9pF, and the matching capacitor is 10pF. The parameters of this crystal cannot be changed at will.

6. 2 Radio frequency related description

6. 2. 1 Conduction

For the chip RF foot, a capacitor is first connected, and then π type or T type matching is used. The matching value should be adjusted according to the actual RF characteristic impedance of the PCBA. For example, refer to circuit C8 and C10.

6. 2. 2 Antenna

It is recommended to reserve π type or T-type matching position, and the matching value should be adjusted according to the actual characteristic impedance of the antenna. For example, refer to circuit C16, R15 and C17.

6. 2. 3 Impedance

The RF impedance line should be impedance controlled at 50Ω.

6. 2. 4 Electrostatic protection

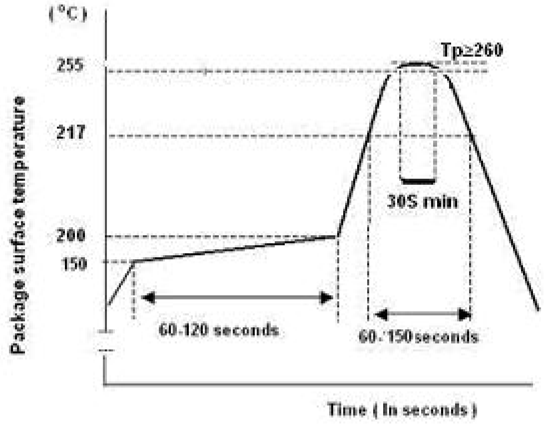
At the antenna inlet, evaluate whether to add ESD protection components based on specific application scenarios. The ESD component's junction capacitance should be ≤1pF. For example, in reference design D7, recommended models include: WAYON WS03DTUF-B, BORN RCLAMP0521P-N, and Taizhou TPESD0508P.

6. 2. 5 Testability

Please evaluate whether it is necessary to design IPEX test seat and production line test disc according to actual requirements.

6. 3 Other application notes

1. CI23242 is manufactured with lead-free and environmentally friendly materials. When SMT welding, please set the furnace temperature and time parameters according to lead-free standards.



2. Attention should be paid to anti-static measures in the process of taking, handling and processing CI23242, and its packaging should be made of anti-static materials.

3. The moisture sensitivity grade of the chip is MSL3. Please store according to the MSL3 condition before use. If the storage time after opening the package exceeds the MSL3 requirement, bake it before SMT soldering.

- Chipintelli reserves the right to interpret and change this specification. If there is any change, we will not give further notice! Customers should obtain the latest version of the data before application design, and verify whether the relevant information is accurate and complete.
- Any semiconductor product may fail or malfunction under certain conditions. The chip application party is responsible for complying with safety standards and taking safety protection measures when using the product for system design and complete machine manufacturing, so as to avoid personal injury or property loss caused by possible product failure!
- Chipintelli will do its best to provide customers with better products and better services!